Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A method of programming a non-volatile memory, the non-volatile memory comprising:

n cell transistors cascaded in series, each cell transistor having a control gate, a floating gate, a source, and a drain;

a local bit line positioned above the n cell transistors, the local bit line being electrically connected to a drain of a 1^{st} cell transistor;

a buried local bit line positioned under the n cell transistors, the buried local bit line being electrically connected to the drain of the 1^{st} cell transistor; and

a source line positioned under the buried local bit line, the source line capable of being electrically connected to a source of a n^{th} cell transistor;

the method comprising:

(a) inputting a word line voltage to a control gate of a k^{th} cell transistor; and

(b) floating the local bit line, and inputting a first source line voltage to the source line for increasing a voltage difference between the control gate of the k^{th} cell transistor and the buried local bit line through capacitance

coupling between the buried local bit line and the source line;

wherein the voltage difference is used to adjust an amount of electrons stored on the floating gate of the k^{th} cell transistor for programming the k^{th} cell transistor.

[c2] 2. The method of claim 1 wherein step (a) further comprises inputting a bit line voltage to the drain of the 1^{st} cell transistor.

[c3] 3. The method of claim 2 wherein step (a) further comprises inputting a second source line voltage to the source line.

[c4] 4. The method of claim 3 wherein the bit line voltage is positive, and the word line voltage is negative.

[c5] 5. The method of claim 4 wherein the first and second source line voltages are positive, and the second source line voltage is less than the first source line voltage.

[c6] 6. The method of claim 1 wherein step (b) raises a voltage level of the buried local bit line, and when the voltage difference between the control gate of the k^{th} cell transistor and the buried local bit line is greater than a predetermined value, the amount of electrons stored on the floating gate of the k^{th} cell transistor is reduced for programming the k^{th} cell transistor.

[c7] 7. The method of claim 1 wherein when an m^{th} cell transistor of the n cell transistors does not needed to be programmed, step (a) further comprises driving a control gate of the m^{th} cell transistor to correspond to a first predetermined voltage, and step (b) further comprises driving the control gate of the m^{th} cell transistor to correspond to a second predetermined voltage, wherein a voltage difference between the second predetermined voltage and the buried local bit line is less than a voltage difference between the first predetermined voltage and the buried local bit line.

[c8] 8. The method of claim 7 wherein the second predetermined voltage is greater than the first predetermined voltage, and the second predetermined voltage is positive.

[c9] 9. The method of claim 8 wherein when the control gate of the m^{th} cell transistor is driven according to the second predetermined voltage instead of the first predetermined voltage, a voltage level of the buried local bit line is accordingly raised owing to capacitance coupling between the buried local bit line and the m^{th} cell transistor.

[c10] 10. The method of claim 1 wherein the non-volatile memory further comprises a main bit line selecting tran-

sistor electrically connected to the drain of the 1st cell transistor and a main bit line, and step (a) further comprises driving the main bit line to correspond to a bit line voltage and turning on the selecting transistor for delivering the bit line voltage to the drain of the 1st cell transistor.

[c11] 11. The method of claim 10 wherein the non-volatile memory further comprises a source line selecting transistor electrically connected to the source of the nth cell transistor and the source line, and the method further comprises turning off the source line selecting transistor.

[c12] 12. The method of claim 11 wherein step (b) floats the local bit line by turning off the main bit line selecting transistor.

[c13] 13. The method of claim 1 wherein the non-volatile memory further comprises r cell transistors cascaded in series, the local bit line positioned above the r cell transistors is electrically connected to a drain of a 1st cell transistor of the r cell transistors, the buried local bit line positioned under the r cell transistors is electrically connected to the drain of the 1st cell transistor of the r cell transistors, the source line is capable of being electrically connected to a source of a rth cell transistor of the r

cell transistors, and when a s^{th} cell transistor does not need to be programmed, step (a) further comprises driving a control gate of the s^{th} cell transistor to correspond to a first predetermined voltage, and step (b) further comprises driving the control gate of the s^{th} cell transistor to correspond to a second predetermined voltage, wherein a voltage difference between the second predetermined voltage and the buried local bit line is less than a voltage difference between the first predetermined voltage and the buried local bit line.

[c14] 14. The method of claim 13 wherein n is equal to r.

[c15] 15. A non-volatile memory capable of implementing the method of claim 1.